## AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) An integrated circuit comprising:

a speed sensing circuit; and

a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers being separated by at least an insulating layer.

2. (Currently amended) The integrated circuit, as recited in claim 1, further comprising:

at least a second capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the second capacitive load being selectively coupled to the first capacitive load, the second capacitive load being formed by at least a portion of an additional metal trace residing in an additional metal layer, the additional metal layer being separated from the first and second metal layers by at least an insulating layer.

3. (Currently amended) The integrated circuit, as recited in claim 1, wherein ~~at least one of~~ the first and second metal layers ~~is a~~ are nonadjacent metal ~~layer~~ layers.

4. (Original) The integrated circuit, as recited in claim 1, wherein at least one of the metal traces has a minimum dimension.

5. (Original) The integrated circuit, as recited in claim 1, wherein at least one of the metal traces has a maximum dimension.

6. (Original) The integrated circuit, as recited in claim 1, wherein at least one of the metal traces has a nominal dimension.

7. (Original) The integrated circuit, as recited in claim 1, wherein at least one of the metal traces is formed as one of a plurality of metal traces having a minimum density.

8. (Original) The integrated circuit, as recited in claim 1, wherein at least one of the metal traces is formed as one of a plurality of metal traces having a maximum density.

9. (Original) The integrated circuit, as recited in claim 1, wherein at least one of the metal traces is formed as one of a plurality of metal traces having a nominal density.

10. (Original) The integrated circuit, as recited in claim 1, wherein the insulating layer has a low dielectric constant (low-k).

11. (Original) The integrated circuit, as recited in claim 1, wherein the speed sensing circuit includes a ring oscillator.

12. (Original) The integrated circuit, as recited in claim 1, wherein the speed sensing circuit includes a resistor.

13. (Currently amended) The integrated circuit, as recited in claim [[1]] 2, wherein the first and second capacitive loads are coupled in series.

14. (Currently amended) The integrated circuit, as recited in claim [[1]] 2, wherein the first and second capacitive loads are coupled in parallel.

15. (Currently amended) The integrated circuit, as recited in claim [[1]] 2, further comprising:

a selective connector selectively coupling at least one of the first and second capacitive loads to the speed sensing circuit.

16. (Original) The integrated circuit, as recited in claim 15, wherein the selective connector includes a fuse.

17. (Original) The integrated circuit, as recited in claim 15, wherein the selective connector includes an anti-fuse.

18. (Currently amended) An integrated circuit comprising:

a speed sensing circuit; and

a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a portion of a second metal trace residing in a second metal layer, the first and second metal layers [[are]] being nonadjacent metal layers.

19. (Currently amended) The integrated circuit, as recited in claim 18, further comprising:

at least a second capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the second capacitive load being selectively coupled to the first capacitive load, the second capacitive load being formed by at least a portion of an additional metal trace residing in an additional metal layer, the additional metal layer being separated from the first and second metal layers by at least an insulating layer.

20. (Withdrawn) A method comprising:

coupling a capacitive load to a speed sensing circuit to measure a delay corresponding to an interconnect structure of an integrated circuit design;

selectively configuring the capacitive load by selectively coupling at least one of a plurality of capacitive structures, the capacitive structures including at least a portion of a plurality of metal layers, the capacitive load being representative of the interconnect structure; and

measuring the delay corresponding to the capacitive load to characterize at least one layer of the interconnect structure.

21. (Withdrawn) The method of claim 20, further comprising:

characterizing the interconnect structure based at least in part on the delay measurement.

22. (Withdrawn) The method of claim 20, wherein at least one of the metal layers is a nonadjacent metal layer.

23. (Withdrawn) The method of claim 20, wherein the delay measurement is based at least in part on a delay of a signal through a speed sensing circuit.

24. (Withdrawn) The method of claim 20, wherein the delay measurement is based at least in part on a frequency of oscillation of a speed sensing circuit.

25. (Withdrawn) The method of claim 20, further comprising:

adjusting a process parameter defining the interconnect structure based at least in part on the characterization.

26. (Withdrawn) The method of claim 20, further comprising:

selectively reconfiguring the capacitive load to be representative of a second interconnect structure of an integrated circuit design; and

measuring a delay corresponding to the reconfigured capacitive load to characterize at least one layer of the second interconnect structure.

27. (Withdrawn) The method of claim 26, further comprising:

characterizing the interconnect structure based at least in part on the measurement.

28. (Withdrawn--Currently amended) A method of manufacturing an integrated circuit comprising:

forming a speed sensing circuit; and

forming a first capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the first capacitive load being selectively coupled to the speed sensing circuit, the first capacitive load being formed by at least a portion of a first metal trace residing in a first metal layer and at least a

portion of a second metal trace residing in a second metal layer, the first and second metal layers being separated by at least an insulating layer.

29. (Withdrawn--Currently amended) The method of manufacturing an integrated circuit, as recited in claim 28, further comprising:

forming at least a second capacitive load for characterizing at least one layer of an interconnect structure in the integrated circuit, the second capacitive load being selectively coupled to the speed sensing circuit, the second capacitive load being formed by at least a portion of an additional metal trace residing in an additional metal layer, the additional metal layer being separated from the first and second metal layers by at least an insulating layer.

30. (Withdrawn--Currently amended) The method of manufacturing an integrated circuit, as recited in claim 28, wherein ~~at least one of~~ the first and second metal layers ~~is a~~ are nonadjacent metal ~~layer~~ layers.

31. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein at least one of the metal traces has a minimum dimension.

32. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein at least one of the metal traces has a maximum dimension.

33. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein at least one of the metal traces has a nominal dimension.

34. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein at least one of the metal traces is formed as one of a plurality of metal traces having a minimum density.

35. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein at least one of the metal traces is formed as one of a plurality of metal traces having a maximum density.

36. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein at least one of the metal traces is formed as one of a plurality of metal traces having a nominal density.

37. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein the insulating layer has a low dielectric constant (low-k).

38. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein the speed sensing circuit includes a ring oscillator.

39. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 28, wherein the speed sensing circuit includes a resistor.

40. (Withdrawn--Currently amended) The method of manufacturing an integrated circuit, as recited in claim [[28]] 29, wherein the first and second capacitive loads are coupled in series.

41. (Withdrawn--Currently amended) The method of manufacturing an integrated circuit, as recited in claim [[28]] 29, wherein the first and second capacitive loads are coupled in parallel.

42. (Withdrawn--Currently amended) The method of manufacturing an integrated circuit, as recited in claim [[28]] 29, further comprising:

forming a selective connector selectively coupling at least one of the first and second capacitive loads to the speed sensing circuit.

43. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 42, wherein the selective connector includes a fuse.

44. (Withdrawn) The method of manufacturing an integrated circuit, as recited in claim 42, wherein the selective connector includes an anti-fuse.

45. (Withdrawn--Currently amended) An apparatus comprising:

means for configuring [[a]] capacitive loads including at least a portion of a plurality of metal layers, the capacitive loads being representative of an interconnect structure of an integrated circuit design; and

means for measuring a delay corresponding to the interconnect structure.

46. (Withdrawn) The apparatus of claim 45, further comprising:

means for reconfiguring the capacitive loads to be representative of another interconnect structure of the integrated circuit.